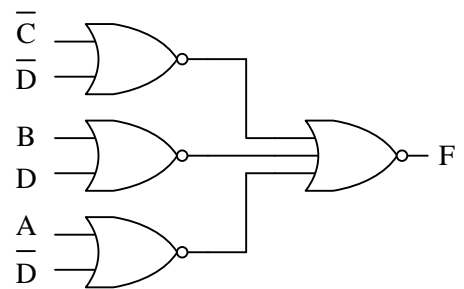


1. $F = (C + \bar{D}) \cdot (\bar{B} + \bar{C})$

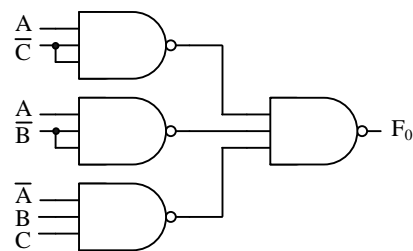
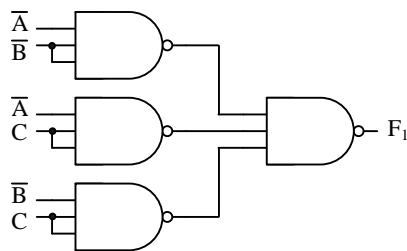
		CD			
		00	01	11	10
AB	00	1	0	1	1
	01	X	0	0	0
	11	1	0	0	X
	10	1	0	X	1

2. $F = (\bar{C} + \bar{D}) \cdot (B + D) \cdot (A + \bar{D})$

		CD			
		00	01	11	10
AB	00	0	0	0	0
	01	1	0	0	1
	11	1	1	0	1
	10	0	1	0	0



3. The functions have to be implemented in NAND-NAND configuration. Implementation using minimize functions require 11 gates : 8 + 3 for the NOT function (\bar{A} , \bar{B} and \bar{C}) \Rightarrow 4 chips.



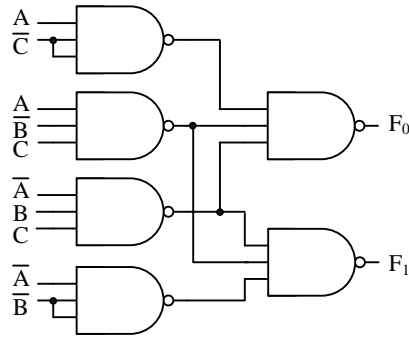
Requires gate sharing

		BC			
		00	01	11	10
A	0	1	1	1	
	1		1		

$$F_1 = \bar{A}\bar{B} + \bar{A}B.C + A\bar{B}C$$

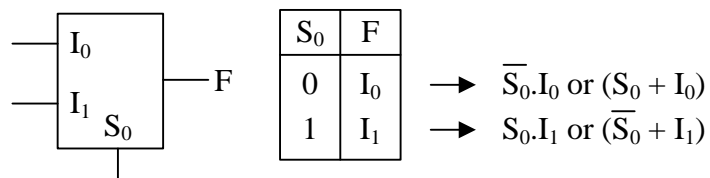
		BC			
		00	01	11	10
A	0			1	
	1	1	1		1

$$F_0 = A\bar{C} + \bar{A}B.C + A\bar{B}C$$

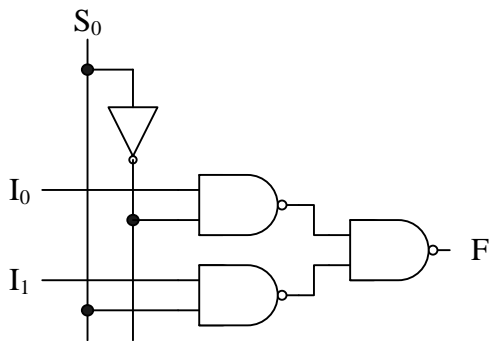


A total of 9 gates : 6 + 3 \Rightarrow 3 chips

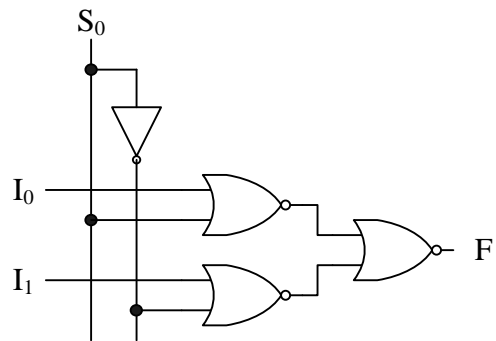
4



$$F = \bar{S}_0 \cdot I_0 + S_0 \cdot I_1$$

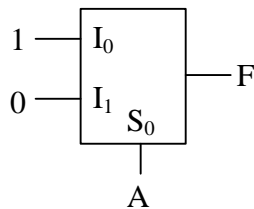


$$F = (S_0 + I_0) \cdot (\bar{S}_0 + I_1)$$



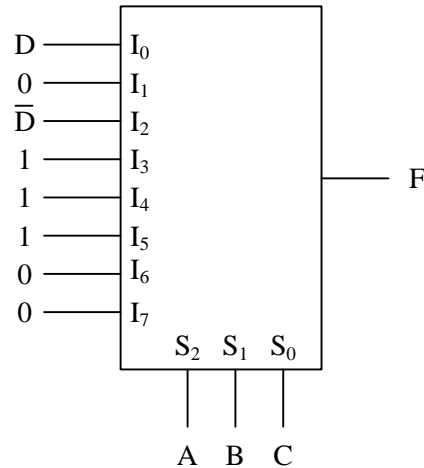
5 (a) $F = A \cdot B$ (And function)

(b)



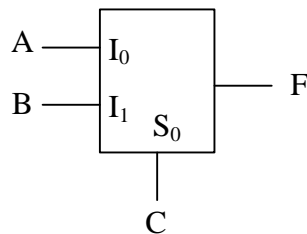
6. (a)

A	B	C	F
0	0	0	D
0	0	1	0
0	1	0	\bar{D}
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0



- (b) (i) The chip is DISABLED.
(ii) The output is taken at pin 6 (complemented output)

7. Implement the function $F(A,B,C) = A\bar{C} + B.C$ using a single 2-to-1 multiplexer without any additional logic gates.

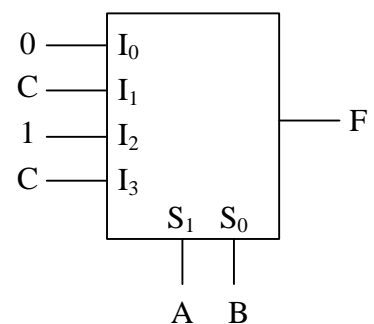


8. $F(A,B,C,D) = \Pi M (3, 9, 11, 12, 13, 14, 15)$

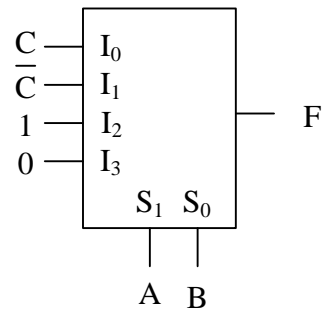
9. A Boolean function $F(A,B,C) = (A+B).\bar{(B+C)}$. Implement the function using a 4-to-1 multiplexer and other logic gates if necessary.

A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

A	B	F
0	0	0
0	1	C
1	0	1
1	1	C



10.



11.

S_1	S_0	a	b	c	d	e	f
0	0	1	1	0	0	1	0
0	1	0	0	1	1	1	0
1	0	0	1	1	0	0	1
1	1	1	0	0	1	0	1

$$a = \overline{S_1} \oplus \overline{S_0}, \quad b = \overline{S_0}, \quad c = S_1 \oplus S_0, \quad d = S_0, \quad e = \overline{S_1}, \quad f = S_1$$

