COURSE OUTLINE

Department & Faculty: Electrical Engineering Faculty	Page : 1 of 4
Course Code: SKEE 1223 Digital Electronics Total Contact Hours: 42 hours	Semester: 2 Academic Session: 2011/2012

Lecturer : MUHAMMAD MUN'IM BIN AHMAD ZABIDI (Section 5)
Room No. : DSP Lab (4th Floor P02) and VeCAD Lab (1st Floor P02)
Telephone No. : 019 777 5303
E-mail : munim@utm.my

Synopsis : This course teaches the fundamental principles of digital systems. From the signal concepts and the importance of numbers systems and codes, it then proceeds to logic gates, their relationship to Boolean algebra and the integration of gates to form complex circuits. The course emphasizes on techniques to design, analyze, plan, and implement simple digital systems using gates and MSI circuits. Simulation software will also be introduced to facilitate learning process.

LEARNING OUTCOMES

At the end of the course, students should be able to:

No.	Course Learning Outcome	Programme Outcome	Taxonomies and Soft-Skills	Assessment Methods
CO1	Explain the signal concept and various number systems and codes used in digital systems.	PO1	C2	HW, Q, F
CO2	Describe the operation of all logic gates, manipulate Boolean Algebra and simplify Boolean functions using Karnaugh Map.	PO1	C2	HW, Q, F
CO3	Differentiate the operation of various MSI circuits and apply them in digital system design.	PO1	C4	HW, Q, F
CO4	Analyze counter and register circuits.	PO3	C4, P4, A2, CTPS1-3	HW, Q, F
CO5	Work in a team and communicate effectively.	PO7, PO9	A3, TS3, LS2	HW
(T – Test ; PR – Project ; Q – Quiz; HW – Homework ; Pr – Presentation; F – Final Exam)				

Prepared by:	Certified by: (Course Panel Head)
Name: Muhammad Arif bin Abdul Rahim Signature: Date: 17 February, 2012	Name: Zulkifli bin Md Yusof Signature: Date:

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STUDENT LEARNING TIME (SLT)

Teaching and Learning Activities	Student Learning Time (hours)
1. Face-to-Face Learning	
a. Lecturer-Centred Learning i. Lecture	36
b. Student-Centred Learning (SCL) i. Laboratory/Tutorial ii. Student-centred learning activities – Active Learning, Project Based Learning	6
2. Self-Directed Learning	
a. Non-face-to-face learning or student-centred learning (SCL) such as manual, assignment, module, e-Learning, etc.	24
b. Revision	24
c. Assessment Preparations	24
3. Formal Assessment	
a. Continuous Assessment (inclusive of presentation)	3.5
b. Final Exam	2.5
Total (SLT)	**120**

TEACHING METHODOLOGY

- Lecture, tutorial and class discussion.
- Group Assignments, Written Quizzes and Final Examination.
- Active learning approach – Group assignment and presentation

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WEEKLY SCHEDULE

Week 1 9.2.14	**Introduction (3 hours)** Differences of analog and digital systems. Analog-digital interfacing
Week 2 16.2.14	**Number systems & digital codes (6 hours)** Conversions between number systems: decimal, binary, hexadecimal, octal.
Week 3 23.2.14	Binary codes: BCD, Gray. Alphanumeric: ASCII, Unicode. Binary arithmetic: +, -, x, /
Week 4 2.3.14	**Gates and Boolean Algebra (3 hours)** Logic gates. Boolean algebra. Boolean theorems.
Week 5 9.3.14	**Combinational Logic Networks (6 hours)** Minterm, maxterm, canonical SOP and POS, don't care conditions, Algebraic simplifications of Boolean functions [Test 1 :. Covers material in week 1 to week 4]
Week 6 16.3.14	Logic simplification using Karnaugh maps, Gate transformations and DeMorgan equivalent circuits
Week 7 23.03.14	**Digital IC (3 hours)** IC classification, CMOS vs TTL, performance characteristics (voltage levels, propagation delay, power dissipation, noise margin, fan-in, fan-out). Datasheets. Glitches and Hazards
Week 8	Mid-Semester Break
Week 9 6.4.14	**Combinational MSI (6 hours)** Multiplexers: concepts, devices (74xl53 and 74xl5l), expansion. Decoders/code converters: concepts, devices (74xl38, 74xl39, 74x47), expansion. Implementations of Boolean functions using multiplexers and decoders
Week 10 13.4.14	Encoders: concepts, devices (74xl48 and 74xl47), expansion. Adders - half adder, full adder, ripple adder, device (74x283). Comparators, device (74x85), Parity generator/checker, device (74x280) [Test 2 : Covers material in week 5 to week 9]
Week 11 20.4.14	**Latches and flip-flops (6 hours)** Differences between combinational and sequential circuits. SR latches, Gated SR latch, Gated D latch,. D flip flop
Week 12 27.4.14	JK flip flop, T flip flop., 74x74 and 74x76 devices. Preset and clear functions. Timing characteristics, timing diagrams.
Week 13 4.5.14	**Sequential MSI (6 hours)** Synchronous and asynchronous counters, ripple counter, 74x293 and 74x163 devices.
Week 14 11.5.14	Register shift registers (SISO, SIPO, PISO, PIPO), shift register counters (Johnson and Ring),74xl64, 74xl65, 74xl94, 74xl95 devices. [Test 3 : Covers material in week 10 to week 13]

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Week 15 14.05.12	**Programmable Logic (3 hours)** PLA, PAL, Memory (RAM, ROM), CPLD, FPGA

REFERENCES :

1. Thomas L. Floyd, "*Digital Fundamentals*" 9h Ed., Prentice Hall, 2007
2. Tocci & Widmer, "*Digital Systems Principles and Applications*", 10th Ed., Prentice Hall, 2007.
3. M. Morris Mano, "*Digital Design*", 4'h Ed. Prentice Hall, 2007.

GRADING:

Item	Mark(%)	No of test/quiz/assignment	Duration
Group Assignments	15	2	
Presentation (Evaluation of TS3, LS2)	5	1	30 mins.
Tests	30	3	3 hours
Final Exam	50	1	2.5 hours

Proposed Dates
Test 1 – 19 March 2014 (Week 6)
Test 2 - 16 April 2014 (Week 10)
Test 3 – 14 May 2014 (Week 14)

All Wednesday nights from 8-10pm. The venues are P16 Dewan Peperiksaan, BKT 3 and BKT 4.