SKEE 1223 DIGITAL ELECTRONICS – 2013/2014 SEM 2
ASSIGNMENT 1

Content / Disciplinary Knowledge :
Boolean algebra, Karnaugh Map, Combinational Logic Design

Generic Skills Tested / Developed:
Communication, Critical Thinking and Problem Solving, Team-working, Leadership, Entrepreneurship Skills, Ethics and Integrity (Based on EPPP)

1. Objective:
(a) Implement a combinational circuit based on your IC number
(b) Simplify and implement your digital design using logic gates.
(c) Simulate the design using Quartus II

2. Specification:
(a) Individual assignment. Your design must have four inputs and four output.
(b) The design can be simplified using Karnaugh map.

3. Project Report:
Your report should include the following:
(a) Project / Product title and names of members on the front cover
(b) Brief description of the problem
(c) Design specifications
(d) Truth table and Karnaugh map
(e) Simulation results
(f) References
(g) Appendix (optional)

4. Marks (20%) - *for late submission, 5% will be deducted
(a) Originality : 2%
(b) Complexity : 2%
(c) Tidiness : 2%
(d) Report : 4%
(e) Punctuality : 5%
(f) Simulation : 5%

5. Important Dates:
(a) Your report MUST be handed in by hardcopy on **28 April 2014 (Monday),** 2pm at P16-BKT1
(b) Please email the softcopy in (***.docx**) to michael@fke.utm.my by **27 April 2014 (Sunday),** 8pm.

NRIC Combinational Circuit Guidelines

NRIC: 830818095193

Any recurring digits replaced with another digit, so it becomes: 830A1BC95DEF

You can also use number that are not in your NRIC

Essentially,

Input 8 -> Output 3
Input 3 -> Output 0
Input 0 -> Output A (hexa for 10)
Input A -> Output 1, and so on.

Create truth table from this, where input (I3, I2, I1, I0) and output (O3,O2,O1,O0) are both 4-bit binary numbers. *Note that there will be don't cares.

I3	I2	I1	I0	O3	O2	O1	O0
0	0	0	0	1	0	1	0
0	0	0	1	1	0	1	1
0	0	1	0	X	X	X	X
0	0	1	1	0	0	0	0
0	1	0	0	X	X	X	X
0	1	0	1	1	1	0	1
0	1	1	0	X	X	X	X
0	1	1	1	X	X	X	X
1	0	0	0	0	0	1	1
1	0	0	1	0	1	0	1
1	0	1	0	0	0	0	1
1	0	1	1	1	1	0	0
1	1	0	0	1	0	0	1
1	1	0	1	1	1	1	0
1	1	1	0	1	1	1	1
1	1	1	1	X	X	X	X

Implement your system according to the configuration below

- O3: NAND-NAND configuration
- O2: NOR-NOR configuration
- O1: Using conventional logic gates
- O0: Using a 4:1 multiplexers and logic gates

For O3, O2, O1 and O0, simplify using Karnaugh map first.

Your front page should be formatted as

NRIC Combinational Circuit

Digital Electronics

SKEE 1223

Section 4

Name IC Matrix Number