UTM
UNIVERSITI TEKNOLOGI MALAYSIA

SKEE1223: Digital Electronics

7 – Digital IC

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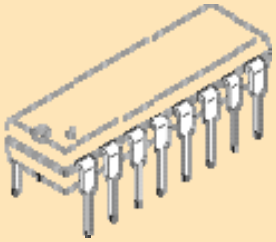
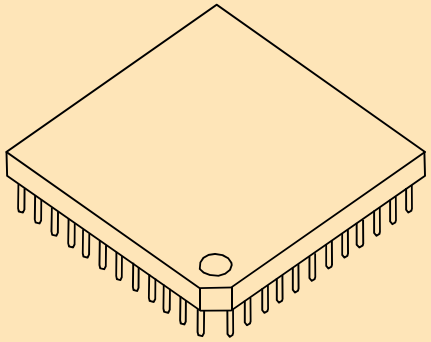
Integrated Circuit

- Known as IC or chip
- Packaged in ceramic or plastic
    1. From 4-6 pins to hundreds
- Pins wired to pads on chip





IC Levels of Integration

Complexity	Number of gates	Example
SSI	≤ 12	Individual gates
MSI	12 – 99	Flip-flops, registers
LSI	100 – 9,999	AVR microcontroller
VLSI	10,000 – 999,999	68000 microprocessor
ULSI	≥ 1,000,000	i7 microprocessor

Logic Families

- **Logic Family** : A collection of different IC's that have similar circuit characteristics
- The circuit design of the basic gate of each logic family is the same
- The most important parameters for evaluating and comparing logic families include:
  - Logic Levels
  - Power Dissipation
  - Propagation delay
  - Noise margin
  - Fan-out (loading)

Example Logic Families

- RTL (*resistor-transistor logic*), DTL (*diode-transistor logic*)
  - Earliest developed
- **TTL** (*transistor-transistor logic*)
  - Still available, used occasionally
  - 7400 series, refined over generations
  - Most rugged – least susceptible to electrical damage
  - Consumes more power than CMOS – not suitable for battery operated devices
- **CMOS** (*complimentary metal-oxide semiconductor*)
  - Lowest power consumption
  - Used to be slow, but fast today
  - Most common logic family – used in all microprocessors
  - Easily damaged by static discharge & voltage spikes
- BiCMOS, ECL, GaAs
  - Speedy, but use more power, more expensive or harder to use

Datasheets

Electrical Parameters etc

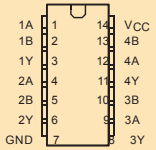
SN5400, SN54LS00, SN54S00 SN7400, SN74LS00, SN74S00
QUADRUPLE 2ĆINPUT POSITIVEĆNANDGATES

SDLS025B – DECEMBER 1983 – REVISED OCTOBER 2003

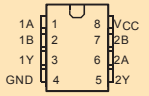
D Package Options Include Plastic Small-Outline (D, NS, PS), Shrink Small-Outline (DB), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) DIPs

D Also Available as Dual 2-Input Positive-NAND Gate in Small-Outline (PS) Package

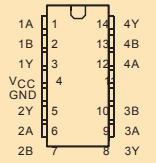
SN5400 . . . J PACKAGE
SN54LS00, SN54S00 . . . J OR W PACKAGE
SN7400, SN74S00 . . . D, N, OR NS PACKAGE
SN74LS00 . . . D, DB, N, OR NS PACKAGE
PACKAGE (TOP VIEW)



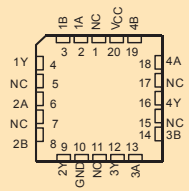
SN74LS00, SN74S00 . . . PS PACKAGE
(TOP VIEW)



SN5400 . . . W PACKAGE
(TOP VIEW)



SN54LS00, SN54S00 . . . FK PACKAGE
(TOP VIEW)



NC − No internal connection

description/ordering information

These devices contain four independent 2-input NAND gates. The devices perform the Boolean function Y = A • B or Y = A + B in positive logic.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conformto specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

- Pinouts
- Packages/Dimensions
- Voltages and Currents
- Noise Margin
- Power Dissipation
- Propagation Delay
- Speed-Power Product
- Fan-In, Fan-Out

DC Supply Voltage

All digital ICs have at least two pins that are connected to the power rails.

	TTL	CMOS
Positive supply voltage	V_{CC}	V_{DD}
Negative supply voltage	GND or V_{EE}	V_{SS}

- For TTL, V_{CC} is +5 V ± 0.5 V.

A TTL gate may be destroyed if the limit is exceeded.

- CMOS gates are tolerant to power supply voltage variations. The power supply ranges from +1.8 V to +18 V. Lower voltage gives better power consumption, a higher value gives faster speed.

Logic Levels

TTL and CMOS use voltages to represent logic levels. Ideally, a single voltage value is specified for each logic level.

V_{CC} (power)	→	Logic 1
GND (ground)	→	Logic 0

In reality, a range of voltages is specified for each logic level.

HIGH Level Electrical Parameters

For a high-state gate driving a second gate, we define:

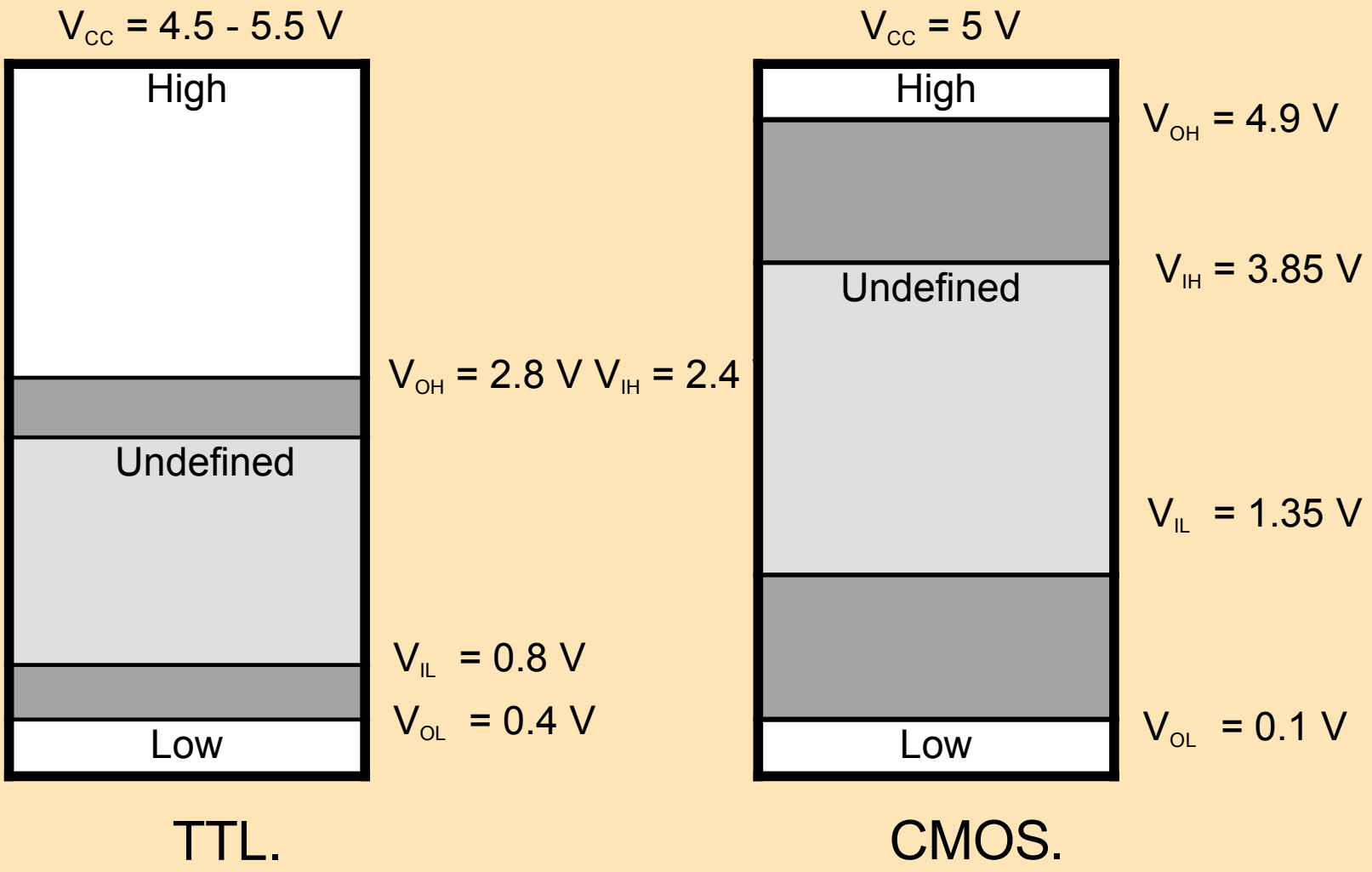
Parameter	Description
V_{OH}	High-level output voltage, the minimum voltage level that a logic gate will produce as a logic 1 output.
V_{IH}	High-level input voltage, the minimum voltage level that a logic gate will recognize as a logic 1 input. Voltage below this level will not be accepted as high.
I_{OH}	High-level output current, current that flows from an output in the logic 1 state under specified load conditions.
I_{IH}	High-level input current, current that flows into an input when a logic 1 voltage is applied to that input.

LOW Level Electrical Parameters

For a low-state gate driving a second gate, we define:

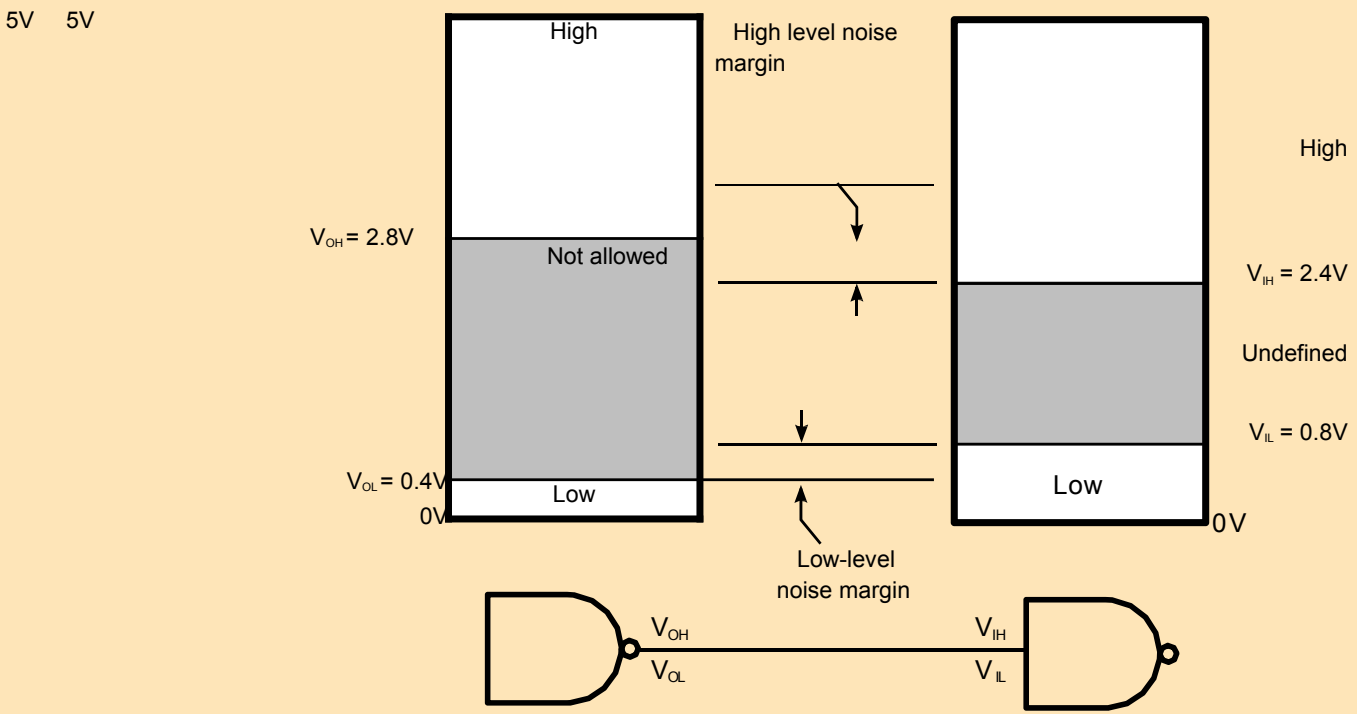
Parameter	Description
V_{OL}	Low-level output voltage, the maximum voltage level that a logic gate will produce as a logic 0 output.
V_{IL}	Low-level input voltage, the maximum voltage level that a logic gate will recognize as a logic 0 input. Voltage below this level will not be accepted as low.
I_{OL}	Low-level output current, current that flows from an output in the logic 0 state under specified load conditions.
I_{IL}	Low-level input current, current that flows into an input when a logic 0 voltage is applied to that input.

TTL vs CMOS Logic Levels



Noise Margin

- If noise in the circuit is high enough it can push a logic 0 up or drop a logic 1 down into the indeterminate or “illegal” region
- **Noise margin** is maximum amount of noise that the circuit can withstand.



Noise Margin

- Noise Margin for logic high is:

$$V_{NH} = V_{OH} - V_{IH}$$

- Noise Margin for logic low is:

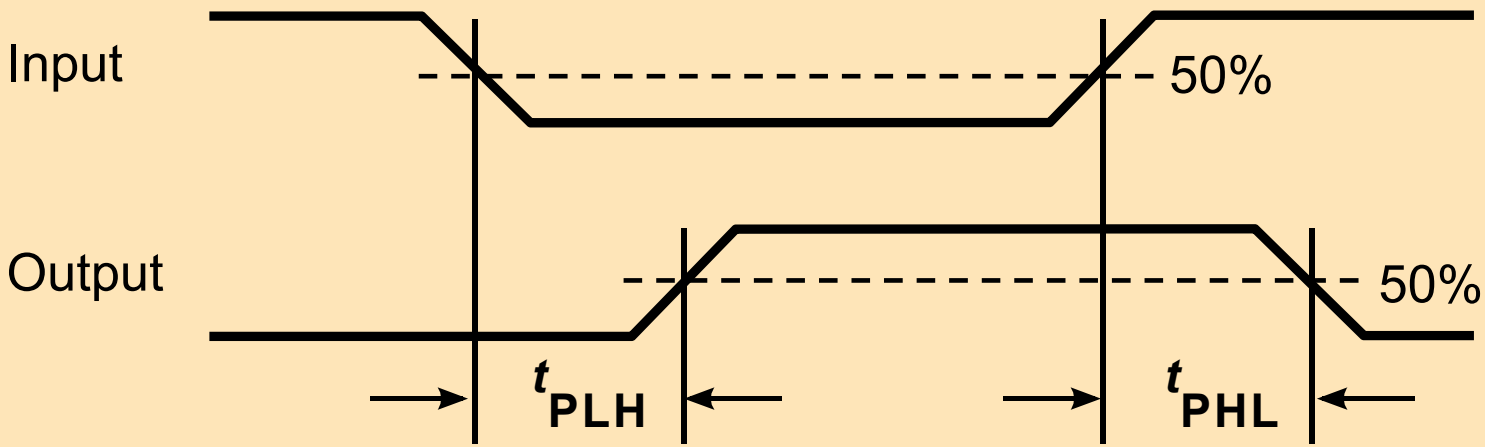
$$V_{NL} = V_{IL} - V_{OL}$$

Propagation Delay

- **Propagation delay** is the delay from a change in input to a change on the output.

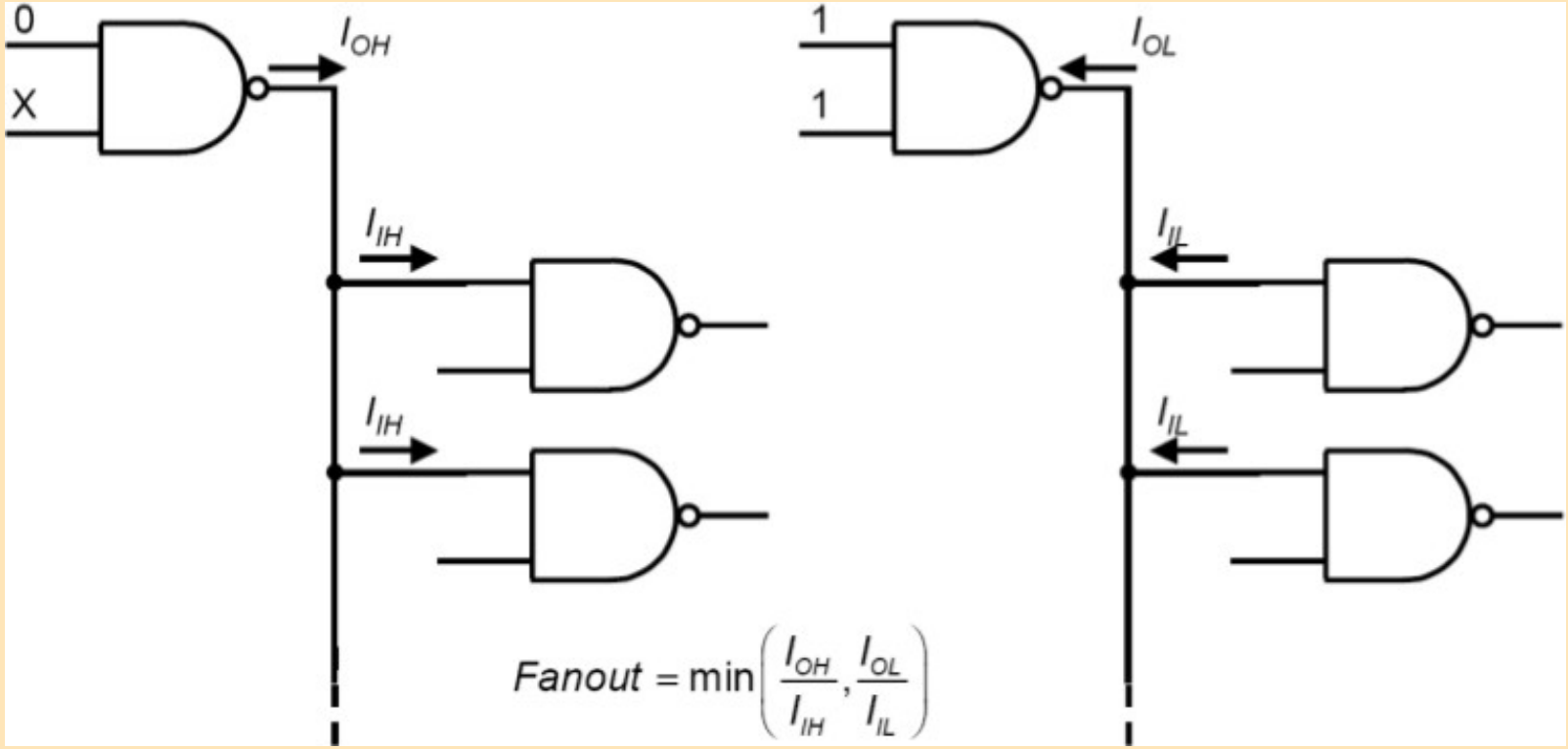
t_{PHL} – delay from an input is given to the time the output changes from high to low.

t_{PLH} – delay from an input is given to the time the output changes from low to high.



Fanout

- The **fanout** is the number of **standard loads** that an output can drive.
- Exceeding the fanout may result in incorrect circuit operation and may destroy the devices

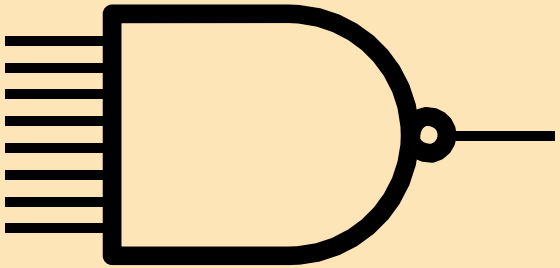


Fanout for CMOS

- Fanout is much higher for CMOS devices than for TTL devices.
- I_{IL} and I_{IH} are extremely small for CMOS (< 1μA).
- Calculating fanout as we did for TTL might yield fanout of 4000 for CMOS, compared to 10 for standard TTL.
- However, increased fanout results in increased delay due to input capacitance.

Fan-In

- Number of input signals to a gate.
  - Not an electrical property
  - Function of the manufacturing process



NAND gate with a fan in of 8.

Power Dissipation

- Static/quiescent
  - Due to passive components
  - No input signal
- Dynamic
  - Due to charging and discharging capacitances through resistances
  - Varies with operating frequency

Speed-Power Product

- Speed (propagation delay) and power consumption are the two most important performance parameters of a digital IC.
- **Speed-power product (SPP)** – a simple means for measuring and comparing the overall performance of an IC family (the smaller, the better).
- Example, an IC has:
  - an average propagation delay of 10 ns
  - an average power dissipation of 5 mW
  - the speed-power product = (10 ns) x (5 mW) = 50 picoJoules (pJ)

SPP of Various Logic Families

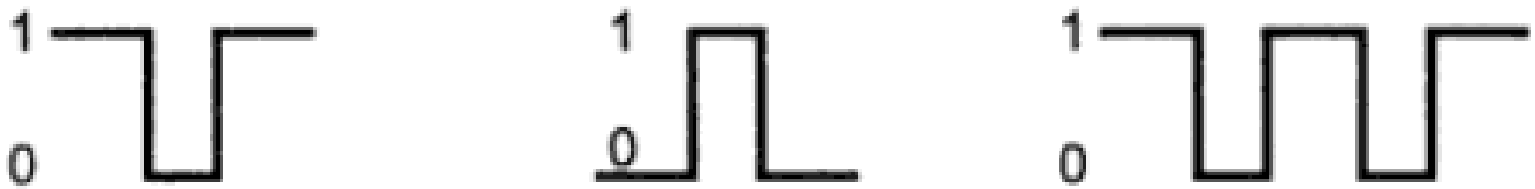
	CMOS		TTL					
	74HC	**4000**	**74**	**74S**	**74LS**	**74AS**	**74ALS**	**74F**
Propagation delay (ns)	8	50	10	3	10	1.5	4	3
Power consumption (mW/gate) Static @ 100 kHz	0.000025 0.17	0.001 0.1	10 10	20 20	2 2	8 8	1 1	4 4
Max clock freq. (MHz)	40	12	35	125	40	200	70	100
Speed-Power Product @ 100 kHz(pJ)	1.4	11	90	60	18	13.6	4.8	12
Fan-Out: LS loads Same series	10 >100	4 >100	40 10	20 20	50 20	20 40	50 20	50 33
Low-level input current (mA)	0.001	0.001	-1.6	-2.0	-0.4	-0.5	-0.2	-0.6

Hazards

Definitions

- A **glitch** is a fast spike.
- A **hazard** is a circuit which may produce a glitch.
- **Static hazard** – a change of a single variable causes a single glitch.
  - Static-0 hazard – Output goes momentarily 1 when it should remain 0
  - Static-1 hazard – Output goes momentarily 0 when it should remain 1
- **Dynamic hazard** – a change in input causes 3 or more transitions when it only be a single 0 → 1 or 0 → 1 transition.

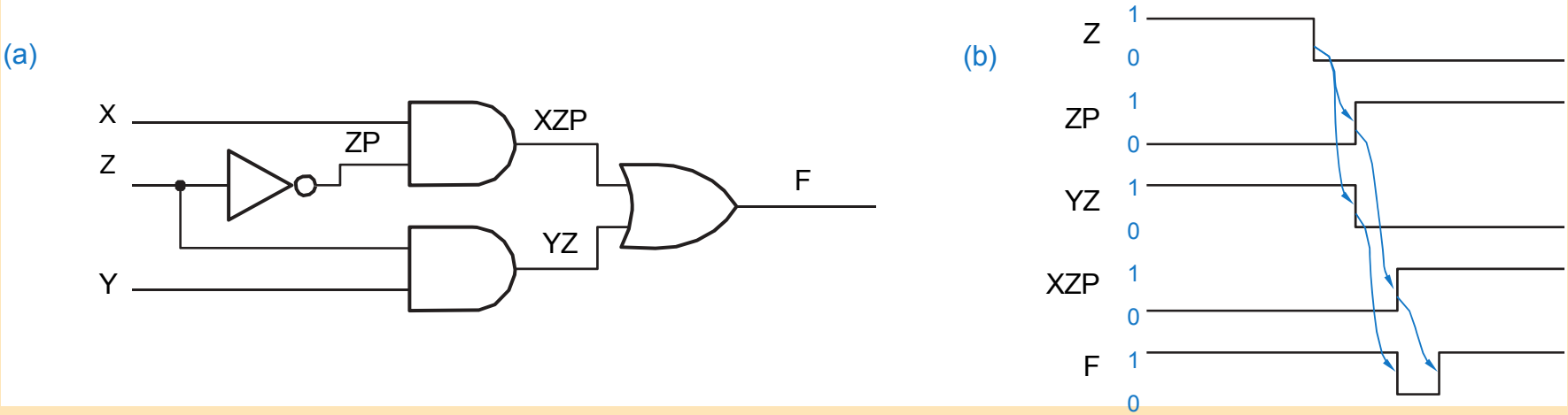
Hazards



(a) Static-1 hazard (b) Static-0 hazard (c) Dynamic hazard

Types of hazards

Circuit with Hazard



Circuit with a static-1 hazard: (a) logic diagram; (b) timing diagram.